**Sr. Embedded Systems Design and Development Engineer**

John C. Westmoreland, P.E.   
  
SUMMARY:   
A highly skilled Electrical Engineering Professional with RF, DOCSIS, networking, embedded system design including MSP430's, MSP430Ware, and FreeRTOS, IC Design of DSPs, FPGA’s and semiconductor wafer-fab experience. Particular expertise in network architecture. Solid track record of taking challenging projects from conception to fruition.   
  
Technical Skills:   
Software: IAR Toolset for MSP-430, ARM, and '8051, TCL/TK, C, CVS, Clearcase, Linux, ClearQuest, Cisco IOS, Ethereal, VxWorks, Xilinx XPS and ISE, Code Composer Studio For MSP430 and TI DSP, Gerbtool, SVN, Cadence Tools Including Allegro and OrCAD, SolidWorks, Pro/E, Altium Designer, Xilinx and Altera FPGA’s (Verilog and VHDL)  
Hardware: Agilent 89441A Vector Signal Analyzer, Spectrum Analyzers, Infiniium Oscilloscopes, Cisco/3Com CMTS's, Wavecom Upconverters, Smartbits, Cisco Routers, LAN-GPIB Gateway, GPIB, Xilinx Virtex-4 FX, LX and CoolRunnerII, BSR-64000, Tektronix 1450  
  
  
PROFESSIONAL EXPERIENCE:

Spring 2020 Projects:  
OWS-451 Replacement For WiFi I/F:  
Designed ESP32 (uBlox NINA) based WiFi Interface to replace deprecated OWS-451 I/F. Schematic capture and PCBA board design done in Altium; ESP32 code development done in Eclipse. Board is currently operational in the Themis design.

Alphanumeric Display and LiIon/Poly Charger for Arduino 33 IoT Series:  
Designed alphanumeric display and Li-Ion/Poly charger for the Arduino 33 IoT family of boards. Schematic capture and PCBA board design done in Altium; application code done in Arduino IDE.

OptiScan Biomedical Corporation, Hayward, CA: Oct. ’18 to Jan. ‘20  
Consulting Electrical Engineer:  
DCP FPGA Test Station Development, including Xilinx ISE (v14.7) on Spartan-3E target; included writing code in Verilog for the Spartan-3E, code for Atmel ARM target (IAR IDE w/Micrium uC/OS-II), and Microchip PIC. Assisting with ongoing board issues and system test of new component selections. PCB/A development/debug using PADS and also using Altium.  
Optiscan’s scanner consists of 27 PCBA’s, all of which were reviewed and updated as necessary for upcoming volume production in 2020.  
Battery charging station and monitor made for OptiScan’s battery system using Arduino MKR CAN I/F’s and MKR Vidor 4000 boards utilizing HDMI out to display battery status.

Altest Corporation, San Jose, CA: Jan.'15 to Dec. ‘19  
Freelance Engineering Consultant: (P/T Basis Only)  
Working with Altest Corporation on various projects including a safety critical project for the transportation industry. Also developed various high speed clock distribution circuits/PCBA’s for major Fotune-100 client; including single-ended and differential. Safety critical project using TI's Hercules family and I developed an industry unique solution for the TPS65381A-Q1 WDOG requirements using TI's HET.

Alter-G, Fremont, CA: Mar 2018 – Mar 2018  
Consulting Electrical Engineer  
Assisted with EMI/EMC related issues; assisted using Spectrum Analyzer and Biconical Antenna to verify. Recommended procedures necessary to help pass FCC/TUV testing. USB 3.0 Based USB cameras also tested.

Complete Genomics Inc., San Jose, CA, Jun 2017 – Jan 2018   
Consulting Electrical Engineer, Hardware and Firmware  
Assisted Complete Genomics with PCBA in their high-speed DNA sequencing system. Board controlled laser, camera, and RTD temperature plus thermal control. Main hardware tool used was Altium; for firmware Keil tools with RTX used.

Equalia LLC, Mountain View, CA, Jun 2017 – Jul 2017  
Consulting Engineer, Firmware  
Assisted with firmware issues regarding Equalia's Hoverboard product (https://www.hoverboard.com/ ) - issues included real-time control and motor-control. Tools used were Altium and IAR EWARM.

Amazon Lab126, Sunnyvale, CA, Sep 2016 – Jan 2017   
Consulting Engineer, RF  
Assisted in RF issues relating to OTA (over-the-air) delivery to offices at Amazon Lab126. ATSC HD Standards regarding OTA implemented in over-the-air delivery system.  
  
AgTech Industries, LLC, Salinas, CA, Jul 2016 – Jan 2017   
Consulting Electrical Engineer, Hardware and Firmware  
Assisted AgTech in hardware design and firmware on their major product line (pending). Main hardware tool used with Altium and for firmware was IAR's EWARM and EW430. Main product contains multiple radio options and OTA bootloader concept was done. Also, MSP430 based TI MAVRK compatible I/F done in some of the product turns. OTA for system updates.

Silicon Constellations, Santa Clara, CA:   
Electrical Engineering Consultant, '15-'16  
Firmware development and consulting on low-power projects and products including some algorithm development.  
  
Alter-G, Fremont, CA: July'13-June'16:  
Electrical Engineering Consultant:  
Assisted with Bionic Leg and AlterG product enhancements.  
  
Spikes Security, Los Gatos, CA Nov.'14-Jan'15  
Electrical Engineering Consultant:  
Internet Security Company; developed proposed architecture and created specification report "Video Hardware (sub)System and CODEC Requirements Specification" Video standards were SD up to 4K: 3840x2160. Some demonstrations done with the DSPC-8682E from Advantech. The DSPC-8682E is based on the TMS320C6678 multi-core fixed and floating point digital signal processor which is based on advanced KeyStone architecture from Texas Instruments. HEVC (H.265) - High Efficiency Video Coding implemented in DSPC-8682E platform as demonstration. Some experimentation done with the EVMK2H from TI/Advantech as well. The EVMK2H has a single 66AK2H14 System on Chip (SoC). The 66AK2H14 is a Multicore DSP+ARM KeyStone II System-on-Chip (SoC) architecture.  
  
Gaderbas Consulting, Alameda, CA: July'12-Jan'14:  
Consulting Electrical Engineer:  
FreeRTOS w/MSP430 based design. Developed BSL loader as well.  
  
Senova Systems, Sunnyvale, CA: August '12-April ‘13:  
Electrical Engineering Consultant, Engineering Department:  
Hardware/firmware work for Senova's pHit solid-state pH meter - responsible for RTOS work  
(FreeRTOS) and assisting in development of converting the existing meter to an RTOS task driven system. Both USB data (including BSL) and Bluetooth (inc. BT 4.0, BLE) capability added to the pHit base system. Hardware work done in Altium Designer. Assisted fellow consulting engineer in the development of pHit Loader and pHit Reports; applications that support BSL loading of the meter and real-time data capture and display.  
  
Tibion Bionic Technologies, Sunnyvale, CA; July '11-July'12:  
Electrical Engineering Consultant/Sr. Electrical Engineer, Engineering Department:  
Hardware/firmware work for Tibion's Bionic Leg. MSP-430 and ARM LPC-2148 firmware and  
hardware work. WiFi (802.11) work. Invensense MPU-6000 Six-axis (gyro + accelerometer) MEMS Motion Tracking Device. Assisted in patent application regarding proprietary communications protocol as well as new sensor technology for bionic leg applications. Developed hardware and firmware prototypes for both. PCBA design done in Altium Designer Release 10.x.  
  
Sanmina-SCI, San Jose, CA; May '10-June '11:  
Sr. Hardware Design Engineer/PM:  
Worked on various projects for large Bay Area Contract Manufacturer; project proposals including RFQ responses; RF Analog Modulator Compliance, Testing, and Validation using Tektronix 1450-1 and TDC-1 including VSWR; DTA for ATSC Free-To-Air Signaling Prototype development, debug and analysis of customer issues, including well known high-end camera system which was done on-site. Project management on all proposals and projects including cost estimation, schedule estimation, BOM costs, prototype costs and production estimate costs and SVN databases. Proposal for FPGA-based PCIe board design.   
High-end camera system included high-speed board design analysis on a multi-board system that includes XAUI, SERDES, I2C, and SPI. Custom ASIC's perform image processing and image capturing tasks. Common-mode noise issues in high-speed environment studied and evaluated in detail. Main control processor is TI OMAP chip.   
  
Motorola, Sunnyvale/Santa Clara, CA: Nov. '08 to Feb. '10:   
Consulting Engineer/Head-End Engineer: Responsible for all head-end operations for OCAP (Open Cable) development group at Motorola - including all RF issues, BSR-64K, DOCSIS, STB's, amplifiers, wiring, configuration, etc. Assisted in defining build-out of new RF/DOCSIS/OCAP lab at Santa Clara site including QA lab.   
  
Teledyne/ISCO San Jose, CA June 2009   
Consulting Engineer:   
FreeRTOS port to MSP430F543X for CCS v3.1 toolset.   
  
Nuvation Research Corporation, San Jose, CA February 2008 to November 2008   
Consulting Electrical/Hardware Engineer:   
Mutil-FPGA high-speed board design including schematic design review and layout supervision/review. Led team of engineers and layout personnel on this project. OrCAD tools with Expedition for layout. Altera Quartus-II FPGA design tools for FPGA work. High-speed signal integrity issues including PCB board material selection. Including board spin.   
  
Microchip Biotechnologies, Pleasanton, CA, May 2008:   
Consulting Engineer - assisted in debug of USB driver issue; including analysis and recommendation for fix.   
  
Proteus Biomedical, Redwood City, CA, August-Sept. 2008:   
Consulting Engineer - assisted in board bring up and debug of MSP-430 and TI DSP based system.   
  
Flextronics Medical, San Jose, CA, Oct. 2007 to Jan. 2008, Sept. 2008 to Nov. 2008   
Consulting Electrical/Hardware Engineer:   
Flex circuit design; board bring up; assistance with Allegro Layout; assembly; schematic capture with Allegro/OrCAD tools; Xilinx CPLD work w/VHDL; TMS320F2812 CCS work.   
Electrical design for new drug application unit, including LCD unit for medical practitioners.   
  
Undisclosed Military Contractor, CA, April 2007 to October 2007   
Consulting Engineer/Firmware/Hardware Engineer:   
Undisclosed government contract. Embedded systems design and development including PCB board design, layout, assembly, bring-up. MSP430 'FG4618 and Silicon Labs 8051. Toolsets for microcontrollers was IAR MSP-430 and IAR 8051.   
  
Primaeva Medical, Inc., Menlo Park, CA January 2007 to April 2007   
Consulting Engineer:   
Developed TEC (Thermoelectric Cooling) Unit for client company product. Custom interface circuitry designed and developed for real-time thermistor measurements. Interface circuitry included buffered high-performance operational amplifiers and digital potentiometers for control. Code done in C and C++. Custom chassis with medical grade isolation and power delivered to client at conclusion of project. Participated in animal study.   
  
Credence Systems, Inc., Sunnyvale, CA December 2006 to January 2007   
Consulting Engineer:   
Assisted in embedded systems design issues of embedded TMS320F2812 DSP-Based microcontroller, including CCS (Code Composer Studio) and DSP/BIOS.   
  
Pentum Group, Inc., Fremont, CA, July 2006 to October 2006   
Consulting Engineer:   
Assisted in initial board bring up of new high-speed board design. Work included basic development with Virtex-4 LX and FX FPGA's. Xilinx XPS and ISE as well as Chipscope used in debug and bring-up. Xilinx Embedded Systems Course certificate earned during this period.   
  
Ecrio Inc., Cupertino, CA, July 2006   
Consulting Engineer   
Design, debug, and automation of discrete transistor white-led (backlight) driver circuit suitable for cell phone displays.   
  
THERASENSE/ABBOTT DIABETES CARE, Alameda, CA April 2005 to May 2006   
Embedded Engineering Firmware Consultant:   
Navigator Sensor Calibration Project -- Assisted in developing new calibration platform for new family of glucose sensors for the Navigator project. Each target board contains 17 TI MSP430's (MSP430F1611IPM) and is able to test 16 sensors simultaneously. Each test platform contains 4 boards. Responsible for all firmware in the project. FreeRTOS (www.FreeRTOS.org) ported to MSP430/IAR for this project. Participated in schematic/design reviews. Development done under Windows 2K/AS using the EW-430 IAR tool suite.   
  
TERAYON COMMUNICATIONS SYSTEMS, Santa Clara, CA August 2004 to Nov. 2004   
  
Lead PQA Engineer:   
· Commercial Services -- Working on commercial services effort -- work has included test equipment evaluation for T1/T3, Jitter and Wander analysis. Have ordered all equipment needed for commercial services test and validation effort.   
· Commercial Services -- beginning to help with characterization which included getting a +48VDC power supply working with an Axerra AXN-800.   
· Euro-DOCSIS -- helped with Euro-DOCSIS testing as needed.   
· DOCSIS PHY and MAC-PHY -- helped with PHY and MAC-PHY testing as needed.   
· GPIB/TCL for Fireberd's -- To help with Commercial Services test automation -- beginning development of a GPIB/TCL library for our Fireberd 6000's.   
· Test Director Evaluation -- began evaluation on Test Director from Mercury Interactive.   
  
LSI LOGIC CORPORATION/C-Cube Microsystems, Milpitas, CA 1999 --2003   
C-Cube Microsystems, acquired by LSI Logic in 2001   
  
Staff Engineer (2000-2003)   
Responsible for DOCSIS ATP certification effort, trade show demonstrations and set-up. Taught training classes.   
· DOCSIS Lab -- Built DOCSIS (Data Over Cable System Interface Specification) lab for Phy and Mac-Phy DOCSIS (cable labs) certification.   
· CVS software repository transition to ClearCase.   
· Wrote Smartbits TCL support library for Phy and Mac-Phy tests.   
· Patent application on proprietary RF (radio frequency) measurement techniques.   
· Wind-River BSP (Board support package) training. Built BSP's to support debug and Wind-View on DVD development systems.   
· Released NET-SNMP-TCL to www.sourceforge.net.   
· Set up and demonstrated our first cable-modem product at Western Cable Show, November 2001 in Los Angeles. Several CM demonstrations set up for CES show. Set up CM demonstration for trade show in UK.   
  
Senior Engineer (1999-2000)   
  
Validation of DAVIC/DVB software running on customer STB's (set-top boxes). Scientific-Atlanta head-end and Divicom (Intersect) head-end responsibility.   
· DOCSIS ECNs (Engineering Change Notices) published by Cable Labs.   
· Certified by Scientific-Atlanta head-end as well as Divicom (Intersect) to work on head-end.   
· Taught hands-on lab on CMTS (Cable-Modem Termination System) basics and cable modem network basics to large groups of engineers at Set-Top Box University   
· Set up, configured, debugged and maintained Scientific-Atlanta head-end for on-site customer, including multi-satellite feed. Trained colleagues on how to use SA head-end.   
  
ON COMMAND CORPORATION, San Jose, CA 1996 -- 1999   
  
Senior Engineer   
· Developed an automated test that exercised the interactive part of Panasonic's server under Lynx OS using pthreads.   
· Assisted in specification of system architecture that is known by the product name OCX.   
· Assisted in bringing video server team up to speed on NT. Developed code under NT as needed, which included porting existing TV network interface code to run under NT.   
  
Next Generation System Hardware Manager   
Acting Hardware Manager for most of next generation platform development; duties included specifying network architecture and tools.   
· Assisted heavily in the field on new system roll-out personally bringing new systems online.   
· Remote management and maintenance specification and development with SNMP (Simple Network Management Protocol).   
· Tested several satellite solutions, including VSAT (Very Small Aperture Terminal).   
· Network specification conformance and test. Engineering lab network responsibility.   
  
Network Engineering Group   
Integral member of Network Engineering Group; including network architecture specification, remote management and maintenance specification and development with SNMP (Simple Network ManagementProtocol), router configuration and specification, VPN (Virtual Private Network) configuration and specification,   
WAN configuration and specification. Also responsible for Engineering Lab Network   
· Began Network Engineering Group -- network architecture specification, RFP (Request for Proposal)publication.   
· Tested several satellite solutions including VSAT (Very Small Aperture Terminal).   
· Assisted in publishing RFP (Request for Proposal) for main ISP and RFP for satellite solution.   
· Assisted with high-speed laptop internet, including cable-modems, an xDSL-like solution and RJ-45 to the rooms. Set up and tested wireless T1 in our Engineering Labs.   
· Working familiarity with TCP/IP Protocol Stack. Working experience with Network General Sniffer and NetXRay.   
· As part of On Command's new system roll-out, assisted heavily in the field, bringing new systems online, including Internet service turn-on. Assisted in setting up and demonstrating new platform at two HITEC shows.   
  
Panasonic Video Server Program Manager   
Responsible for all aspects of system.   
· MPEG-2 conformance and compliance testing.   
· Host and client computer specification and conformance   
· Network specification and conformance and test   
  
INTERACTIVE FLIGHT TECHNOLOGIES, INC. (start-up company), Phoenix, AZ 1995 -- 1996   
Embedded Systems Group Team Leader   
Major projects were second generation VOD (Video-on-Demand) server and real-time audio processing DSP design. Responsible for small group of direct-hire engineers, plus a small team of engineering contractors.   
Responsible for getting first generation VOD server stable by developing good, solid code. Managed all aspects of new designs as well as support of existing designs in field.   
· VOD (Video-on-Demand) hardware debug and firmware development. Second generation VOD architecture and DSP-based BTSC CODEC.   
· Windows-NT programming of two arcade-style games to satisfy contractual requirements.   
Tools used:   
WorkView Office for NT for schematic capture   
MAX PLUS-II tools from Altera under NT for FPGA Development   
Embedded Performance Tools Including SYS-29K Panther Emulator and all associated tools   
Microsoft C/C++ 4.2 under NT   
SoftIce for NT   
TI DSP tools   
Analog Devices SHARC Tools   
Technologies in System: MPEG, RAID, SCSI, RS-485, NTSC, RISC, DSP, FPGA, EPLD, FLASH   
  
TELESOFT INTERNATIONAL, INC. (ISDN start-up), Austin, TX 1994 -- 1995   
TeleSoft International, Inc. is a hardware and software solutions provider for BRI and PRI ISDN   
Senior Engineer   
Responsible for existing hardware designs as well as developing new ones. FPGA design using XACT from Xilinx and ProSeries from ViewLogic. Responsible for LLD's and other ISDN-related software. Current designs are PCAT compatible cards.   
· Developed 68302 based U-Interface ISDN NT1 TA and responsible for S/T design. Demonstrated at Comdex.   
· Design and layout in P-CAD. Certified in P-CAD.   
Environment: Development work and layout done on Pentium-based PCs.   
  
NUTS TECHNOLOGIES, LTD., (Video Conferencing start-up), Hong Kong 1993 -- 1994   
A video-conferencing solutions provider for both PC and MAC   
Design Engineer, Hardware Design Group Responsible for design of AMD 29K-based ISDN stand-alone system and PC-based ISDN TA; including schematic entry using ViewLogic and OrCad, PCB NetList Generation for Mentor PCB Tools on the Sun workstation, ICE (In-Circuit Emulation) using the SYS-29K PUMA, ISDN Software Portation and Integration, ISDN Debug and Analysis with Protocol Analyzer, Real-Time Operating System (RTOS) (Nucleus) Development and Debug, SCSI Software Portation and Integration, System Checkout and Debug, ISDN Certification and Compliancy, Make Ready for Market   
· Design of and 29K-based ISDN stand-alone system and PC-based ISDN TA (terminal adapter).   
· First board developed was combination stand-alone/MAC Nu-Bus card. All subsequent boards were PC-AT compatible.   
· Assisted in Audio 'C31-based CODEC development as needed.   
Environment: Development work done on '486-based PCs. PCB Layout done on Sun workstations.   
  
TEXAS INSTRUMENTS, INC., Stafford, TX 1988 -- 1993   
Electrical Design Engineer, Semiconductor Group (1991--1993)   
Worked in floating-point DSP design group on 'C4X, 'C3X and 'C1X designs   
· 320C40 pDSP (p is for parallel): worked on software support and fault grading issues.   
· 320C41 (320C40 Spin): Set up logic design databases, modified simulation model and test cases; ran regression. Required 'C4X assembly test case modification. Test cases included functional, functional fault and JTAG.   
· 320C31 "Compaction": Set up logic design databases, ran original regression and worked on new timer cell. Debugged and logic validated timer cell. Supported PG regression. Worked on TLM (Triple Level Metal) routing issues.   
· 320C31: Assisted customers in getting simulation model up and running.   
· 'C1X: Evaluated first generation issues.   
Software: Software simulation tool analysis and evaluated software tools.   
Environment: Apollo DN4500's, HP 400's and Sun workstations and servers; running BSD 4.3 compatible UNIX and X-Windows. BSD 4.3, System 5.3 and AEGIS C and C-Shell script Programming.   
  
Software Systems Engineer, Computer Video Products (1990--1991)   
Worked with TIGA (Texas Instruments Graphics Architecture) developing software for TI's family of GSP's (Graphics System Processors). Developed assembly and C DLL's (dynamic-link libraries) for Windows as well as numerous TIGA/Windows demonstration programs. Worked on the TIGA device driver for Windows.   
Investigated Windows Multi-Media extensions.   
· Developed TIGA/Windows 3-D Real-Time 34020/34082 Demo Program, released in 34082 3-D library package.   
· Wrote TIGA/Windows application note, published in Users Guide.   
· Developed software enabling one program to call multiple TIGA boards in system.   
  
Test Equipment Engineer, Dallas, TX (1988--1990)   
Dallas Linear-II wafer FAB which manufactures volume linear products such as the TL074 Operational Amplifier.   
Projects included an automatic visual inspection system for wafer defect detection and keeping the Dallas Linear-II Multiprobe Environment running. Supervised two technicians as direct reports; helped select and train two   
engineers hired to work on Automatic Visual Inspection System Project. Familiar with wafer-fab semiconductor processing and manufacturing as well as digital image processing   
· Chief Systems Engineer for Automatic Visual Inspection system. Wrote C language control program. Automatic Visual Inspection System uses Cognex Vision system to do digital image processing as well as peripheral functions in system.   
· Began program for rewriting operating system software on ATE (Automated test equipment) in the Dallas Linear-II multiprobe area.   
Environment: '386-based PC software development; including C programming, 80x86-based assembly, Basic, z80 assembly, 8080 assembly. Set up SCO Unix on '386 systems. Some Sun and IBM 370 programming.   
  
OTHER RELEVANT EXPERIENCE:   
  
Bay Area Software Tools Developer:   
Assisted in developing high-speed download development solution for ARM (Advanced RISC Machines) Embedded Systems Development.   
  
Bay Area Embedded Tools Developer:   
Developed ARM-based embedded systems emulation solution including Ethernet interface.

Volunteer ExaminerSilicon Valley Volunteer Examiners for the ARRL  
Jun 2012 – Present  
I periodically volunteer to help with Ham radio licensing examinations as a VE - volunteer examiner. I help when I can in the Silicon Valley area.  
I have also assisted with on-site licensing exams at the local Bay Area Maker Faire - I was the assistant VE admin. for Maker Faire 2017 and am the VE admin. for 2018 Maker Faire in San Mateo on May 18th, 19th, and 20th.

EDUCATION   
University of California at Santa Cruz, Santa Cruz, CA – was enrolled in MSCE Program Specializing in Network Engineering; was also enrolled in SCPD program   
B.S., Electrical Engineering, Lamar University, Beaumont, TX   
Eta Kappa Nu, Tau Beta Pi, Pi Mu Epsilon, Phi Kappa Phi, Dean's List, President's List   
SMU -- completed 15 hours toward MSEE   
  
COOPERATIVE EDUCATION EXPERIENCE: Dow Chemical USA (1 semester) and Gulf State Utilities (3 semesters)   
· Programming assignments: Wrote communications program for HP 9000 Series 217 workstation, Modifying DIBINT (distance, bearing, intersection FORTRAN program) including Andoyer-Lambert Subroutine (took into account curvature of the earth).   
· Solid-state emergency horn (hardware and firmware design) control for major chemical company;   
· Power-factor correction and communication control systems for electrical utility company.   
  
In early ‘80’s – US Merchant Marine experience (engine room) plus worked at Bethlehem Steel one summer as rigger.

PATENT   
US Patent #05325071, "Operational amplifier with digitally programmable gain circuitry on the same chip."

Pending Application: US20130165817A1 “Orthotic device sensor.”

PROFESSIONAL ASSOCIATIONS   
· Passed EIT in April 1988; EIT #ET-28012 (TX); Passed the Principles and Practice Examination October 2001. CA EE License #16612. Established NCEES Council Record July 2002. USCIEP Registry Established December 2002.   
· Past CSPE Santa Clara Valley Chapter President & State Director. Member: IEEE, ACM, SAME, AEA, NSPE, CSPE. NFPA Electrical Section member.   
· ARRL Member - AJ6BC (KJ6HCV) - Ham Radio Amateur Extra License