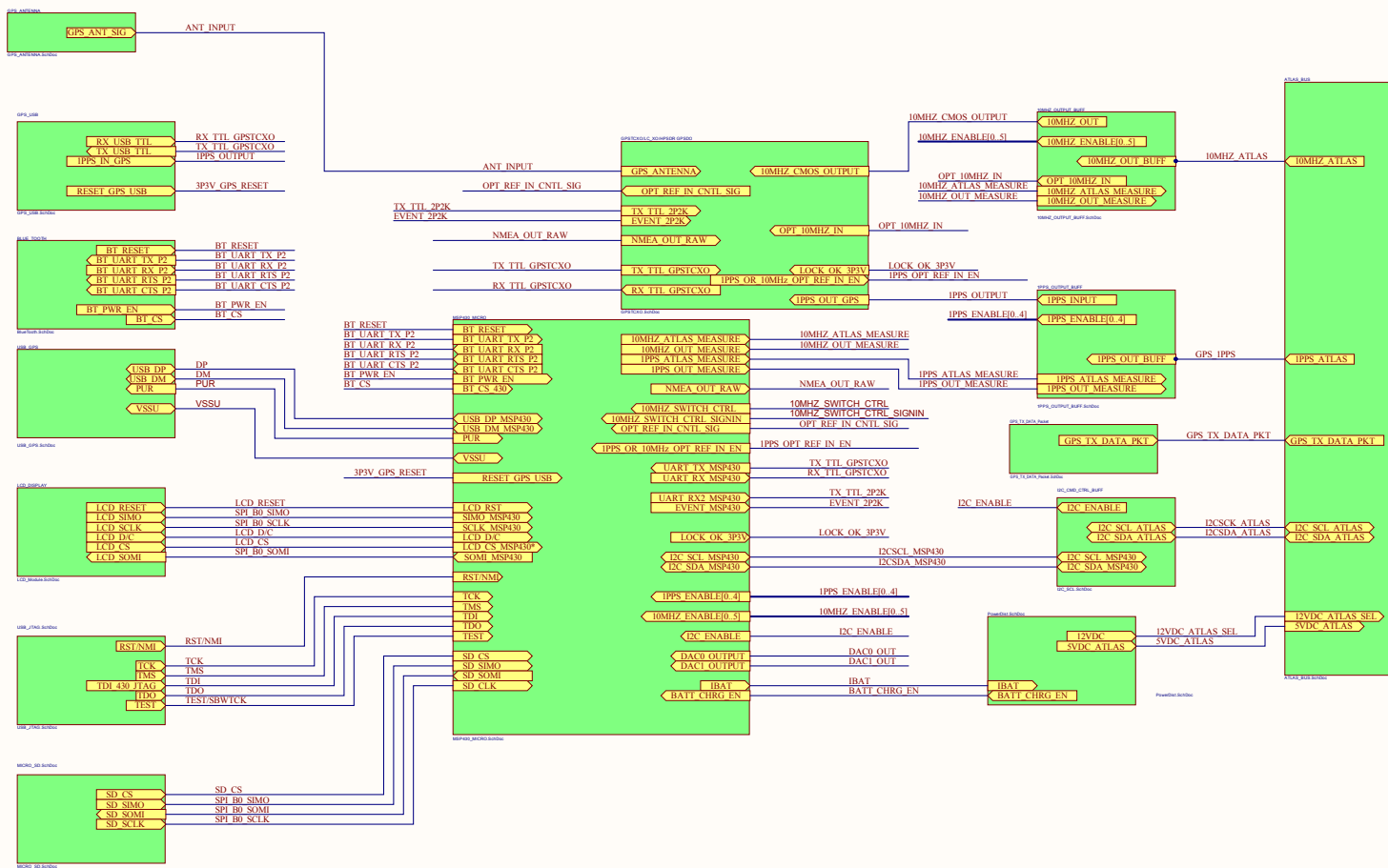


KHRONOS BLOCK DIAGRAM



Note: Preliminary Schematic Release - May 10, 2014 - AJ6BC

Preliminary Schematic
Release - May 10, 2014 -
AJ6BC



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Project: KHRONOS
Author: John West
Date: May 10, 2014

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KHRONOS BLOCK DIAGRAM

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KHRONOS BLOCK DIAGRAM

KHRONOS BLOCK DIAGRAM

KHRONOS BLOCK DIAGRAM

KHRONOS BLOCK DIAGRAM

KHRONOS BLOCK DIAGRAM

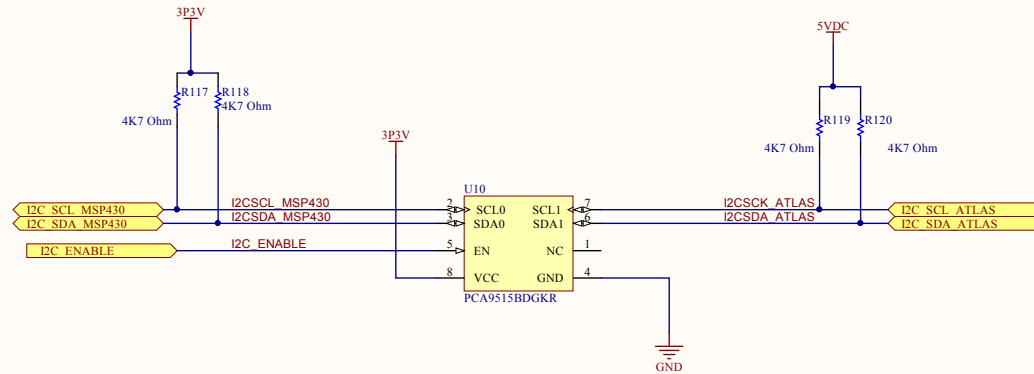
KHRONOS BLOCK DIAGRAM

KHRONOS BLOCK DIAGRAM

KHRONOS BLOCK DIAGRAM

KHRONOS BLOCK DIAGRAM

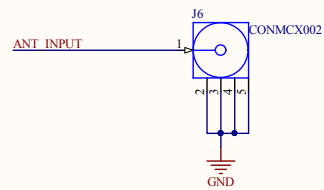
5V Tolerant I2C I/F



		#000PSCB #000PSCB: JOHN WESTMORELAND - ASBC #00LHARMAN - VMSM For Latest Updates: Refer To: http://openhpsdr.org/wiki/index.php?title=000PSCB	
		I2C COMMAND AND CONTROL BUFFER	
Drawn By: John Westmoreland	Date:	CAGE Code:	DWG NO: I2C COMMAND AND CONTROL R01
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GPS ANTENNA INPUT

GPS_ANT_SIG ANT_INPUT



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ENGRS: JOHN WESTMORELAND - AJ68C

PHIL HARMAN - VKEPH

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<http://www.fishbase.org>

Refer To: <http://openhpsdr.org/wiki/index.php?title=GSPSTCRO>

GPS ANTENNA INPUT

Size

CAGE Code	
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DWG NO	
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GPS-ANTENNA-INPUT-RA01

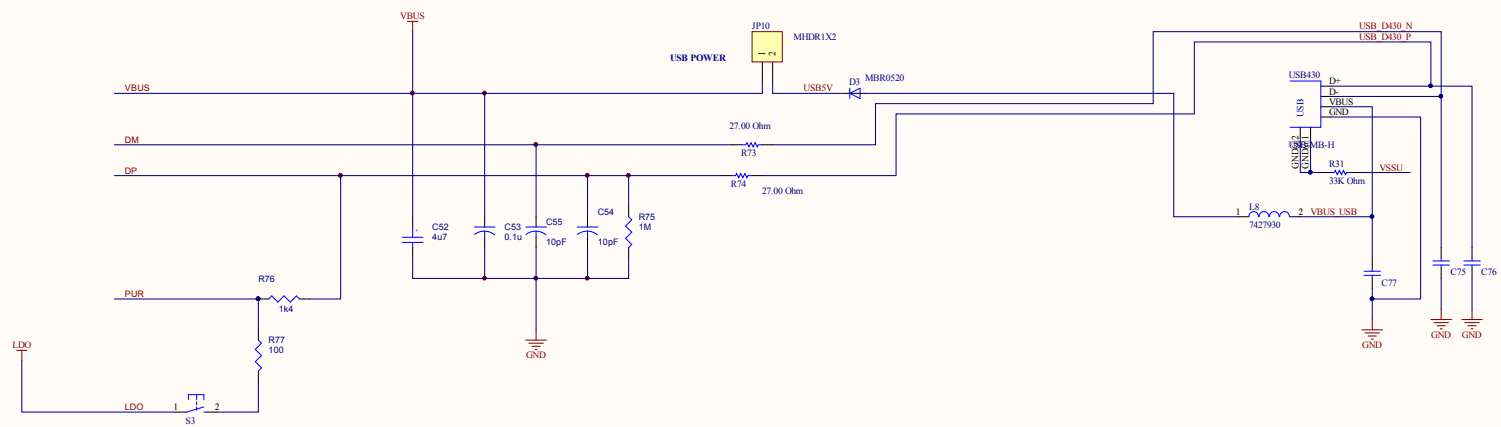
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Scale

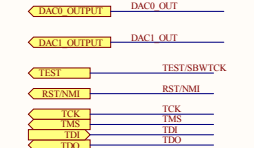
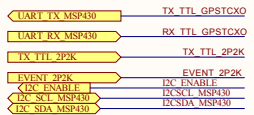
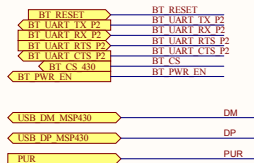
Date(Preliminary Schematic Release): May 10, 2014

59

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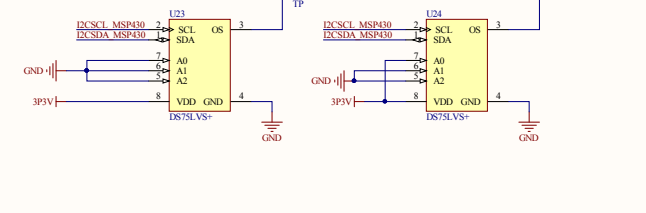
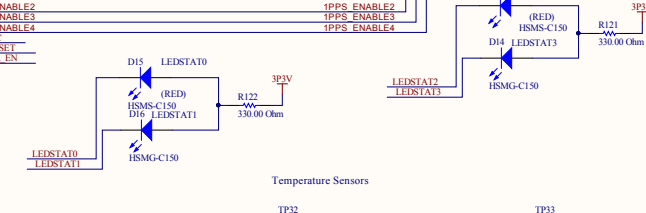
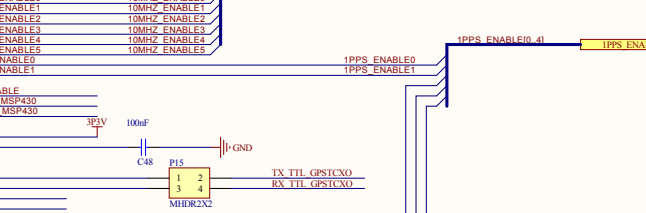
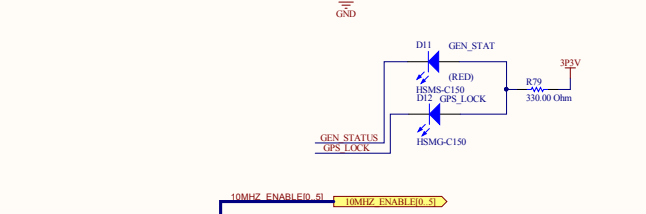
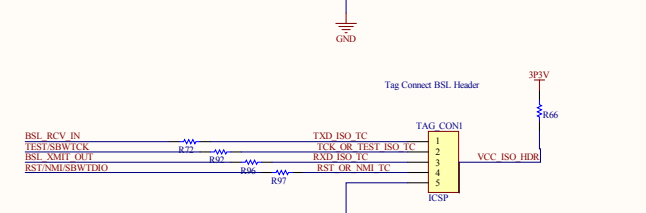
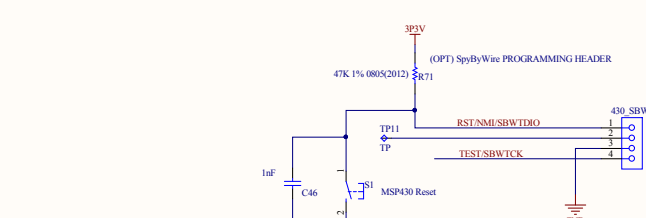
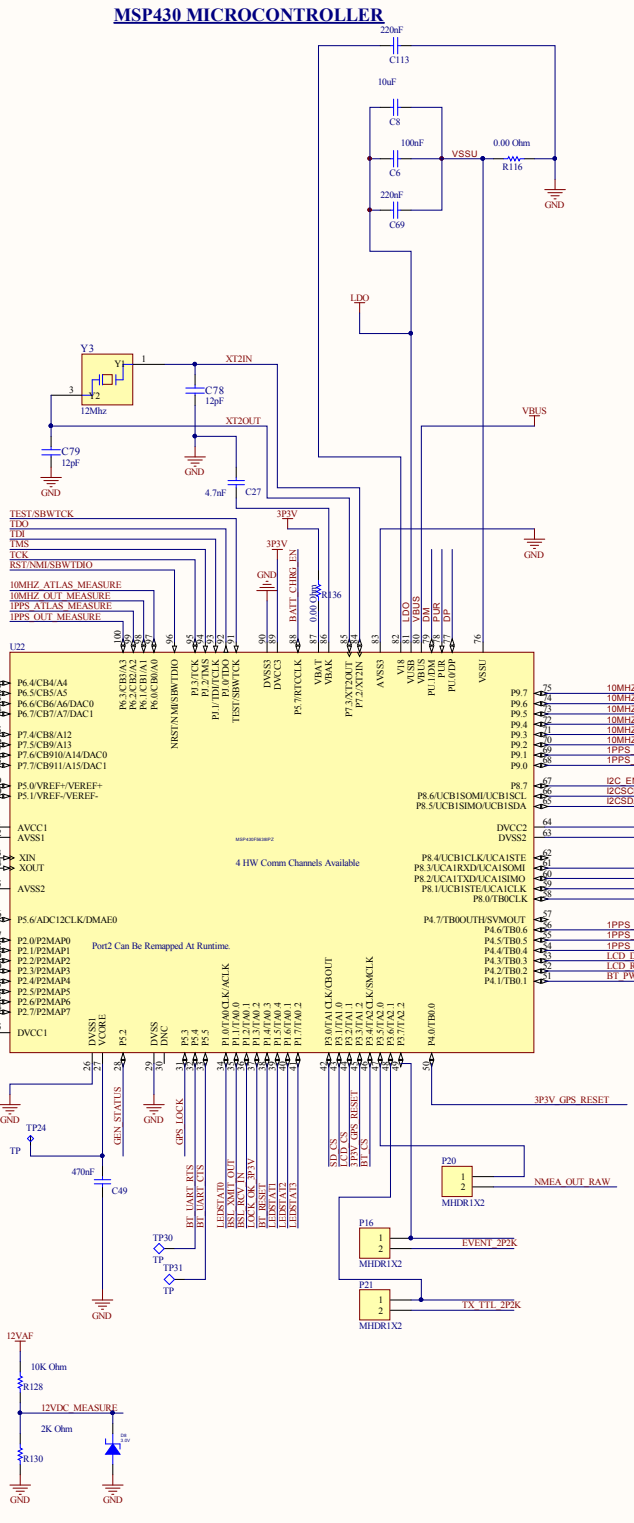
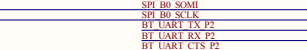
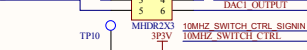
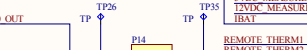
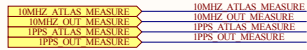
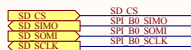
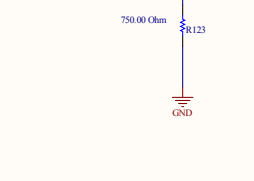
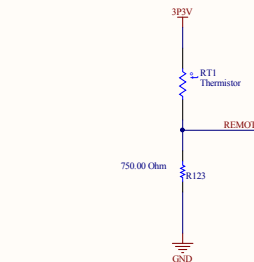


MSP430 MICROCONTROLLER



Comm Channel Assignments:
ATLAS I2C: - UCBI
BlueTooth: UART (default), SPI, I2C
microSD: SPIx
LCD: I2C, SPI, or UART
GPS: Has to be a UART

Remote Temperature Sensing



openHPSDR

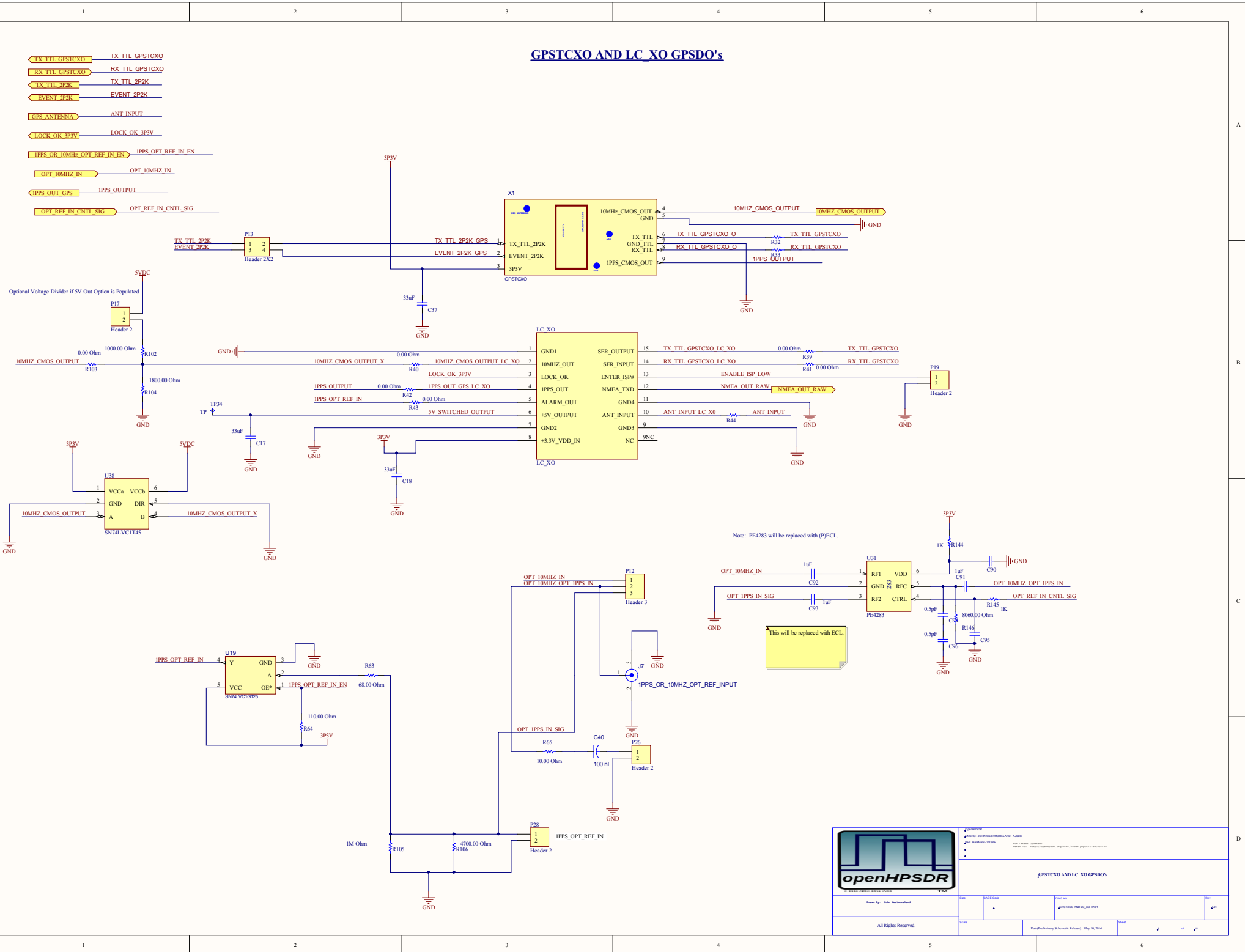
MSP430 MICROCONTROLLER

Version: 1.00 (2020-01-01)

Author: [Name]

License: [License]

Copyright: [Copyright]

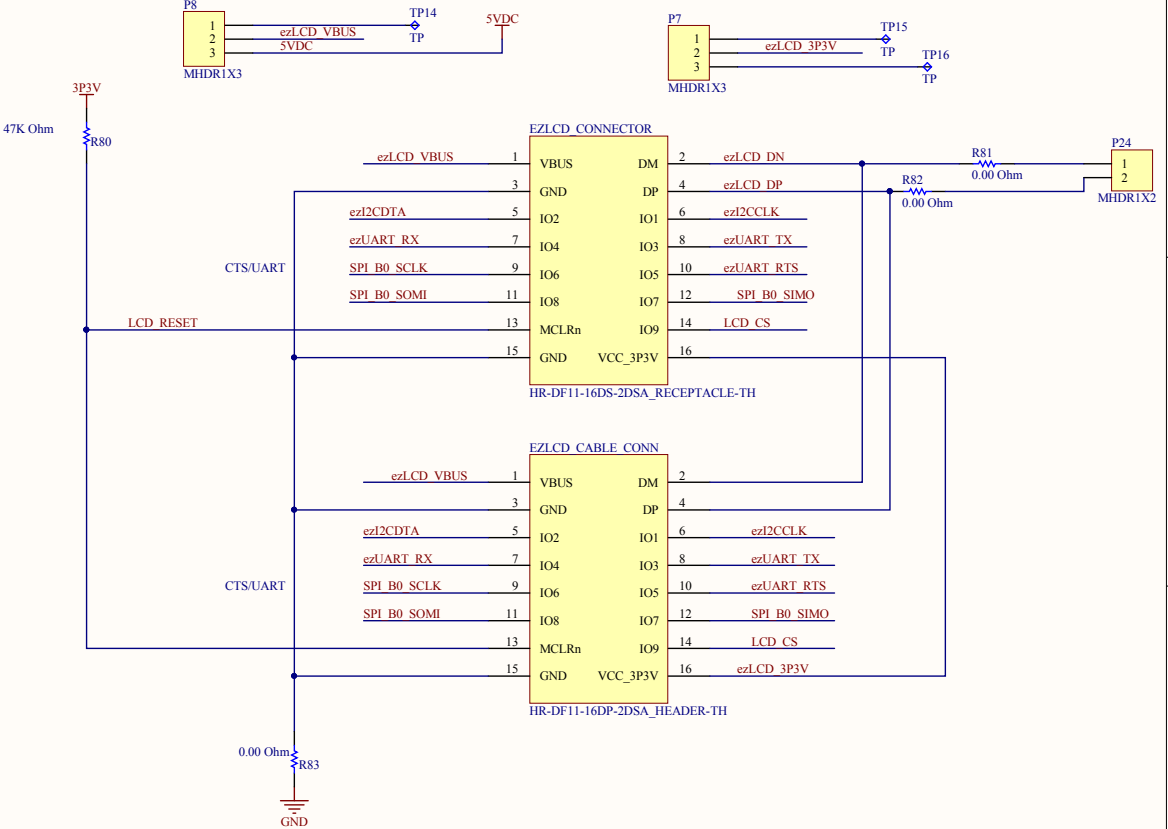
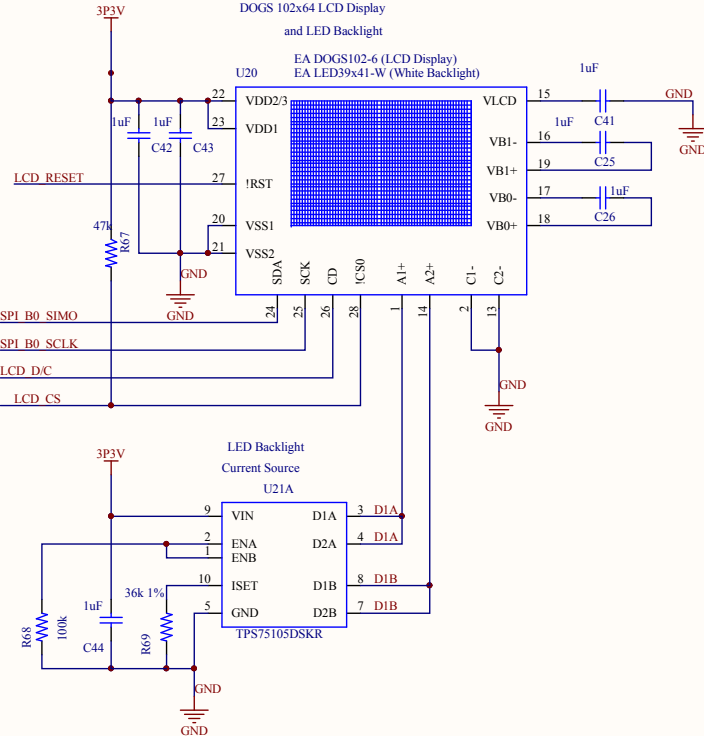


LCD MODULE AND INTERFACE



Note these can go to P2 on the 430 that can be remapped.

Optional EA or ezLCD Displays



Can optionally use DF11-16DP-2DS: RT ANGLE HDR

Connector Board Orientation: Pin 1 on 'Bottom'

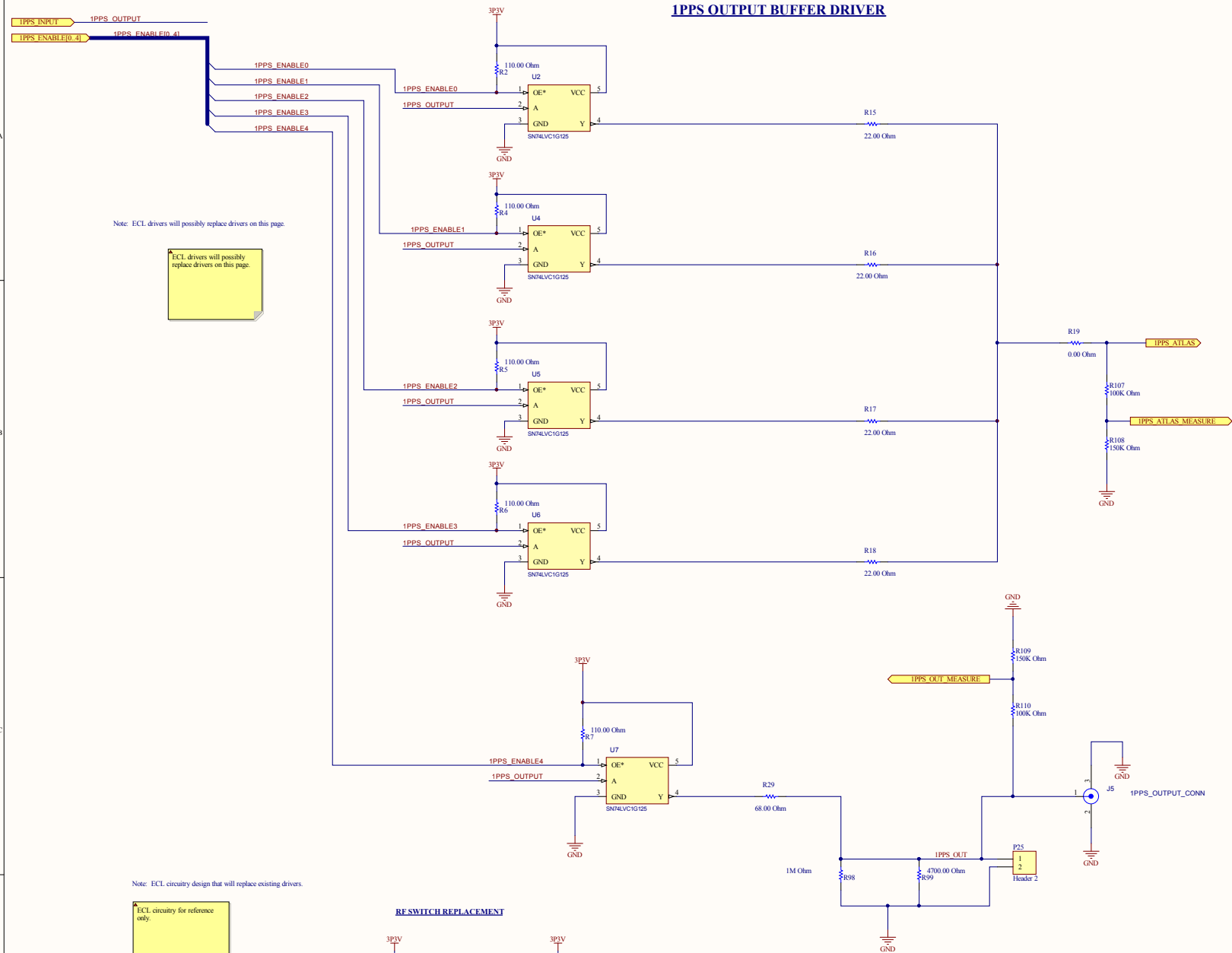


LCD MODULE AND INTERFACE

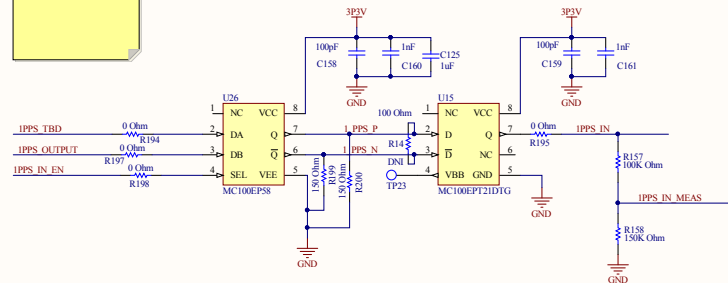
Drawn By: John Westmoreland

LCD-MODULE-AND-INTERFACE-RA01

1PPS OUTPUT BUFFER DRIVER



RE SWITCH REPLACEMENT



#OpenPSDR
 @NGR: JOHN WESTMORELAND - JWH6C
 PHIL HORDEN - VYKPH For Latest Updates:
 Refer To: <https://opendpsdr.org/wiki/index.php?title=CONTRIBUTORS>

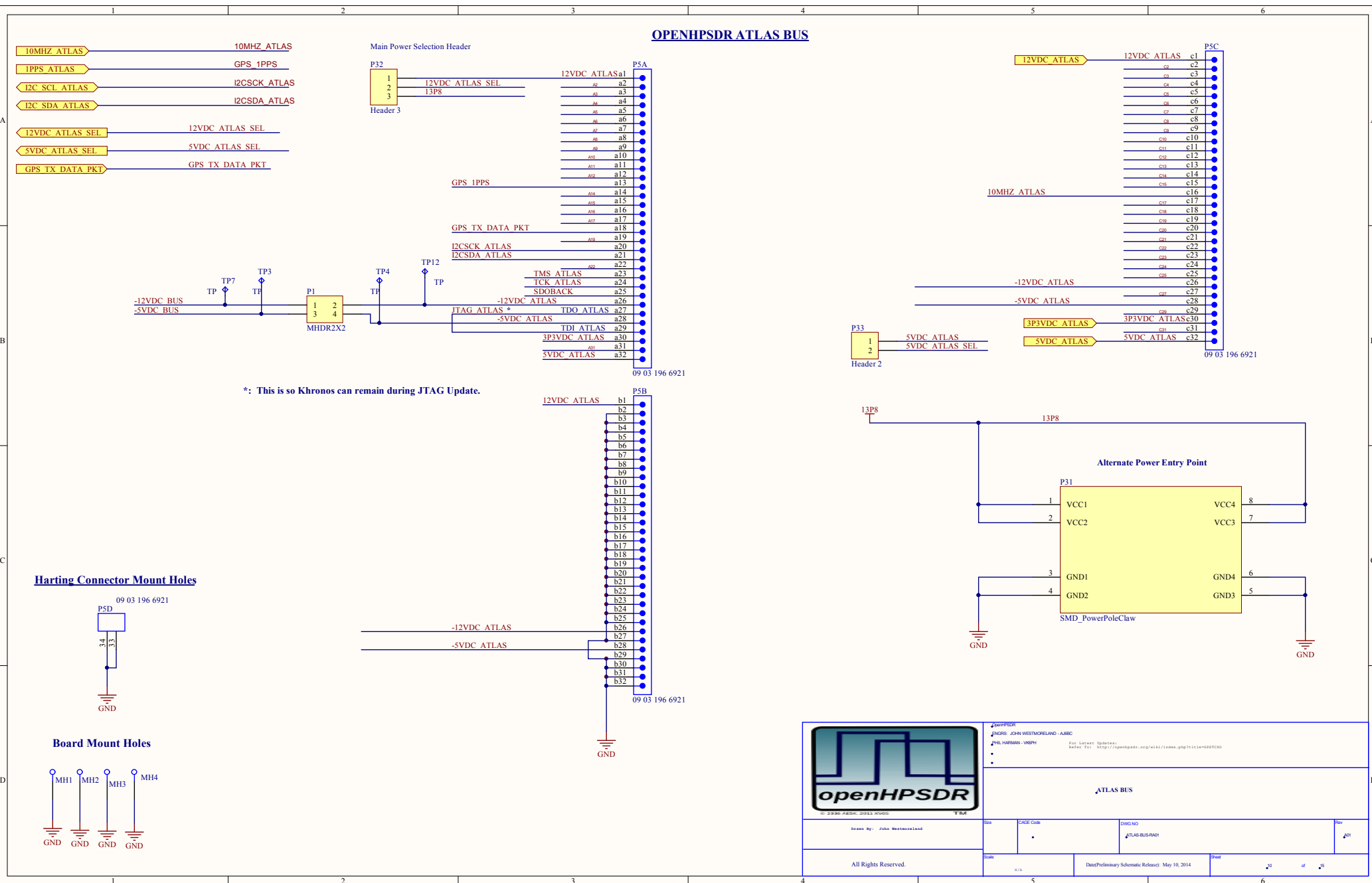
1PPS OUTPUT BUFFER

Team By: John Westermarck

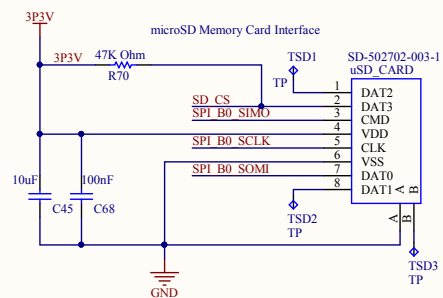
Size	CASE Code	DWG NO
	•	•

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DasPolimery Schematiki Ekzami: May 11, 2014



SD CS	SD CS
SD SIMO	SPI B0 SIMO
SD SOMI	SPI B0 SOMI
SD SCLK	SPI B0 SCLK



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ENGRS: JOHN WESTMORELAND - AJ69C
PHIL HARMAN - WKBP
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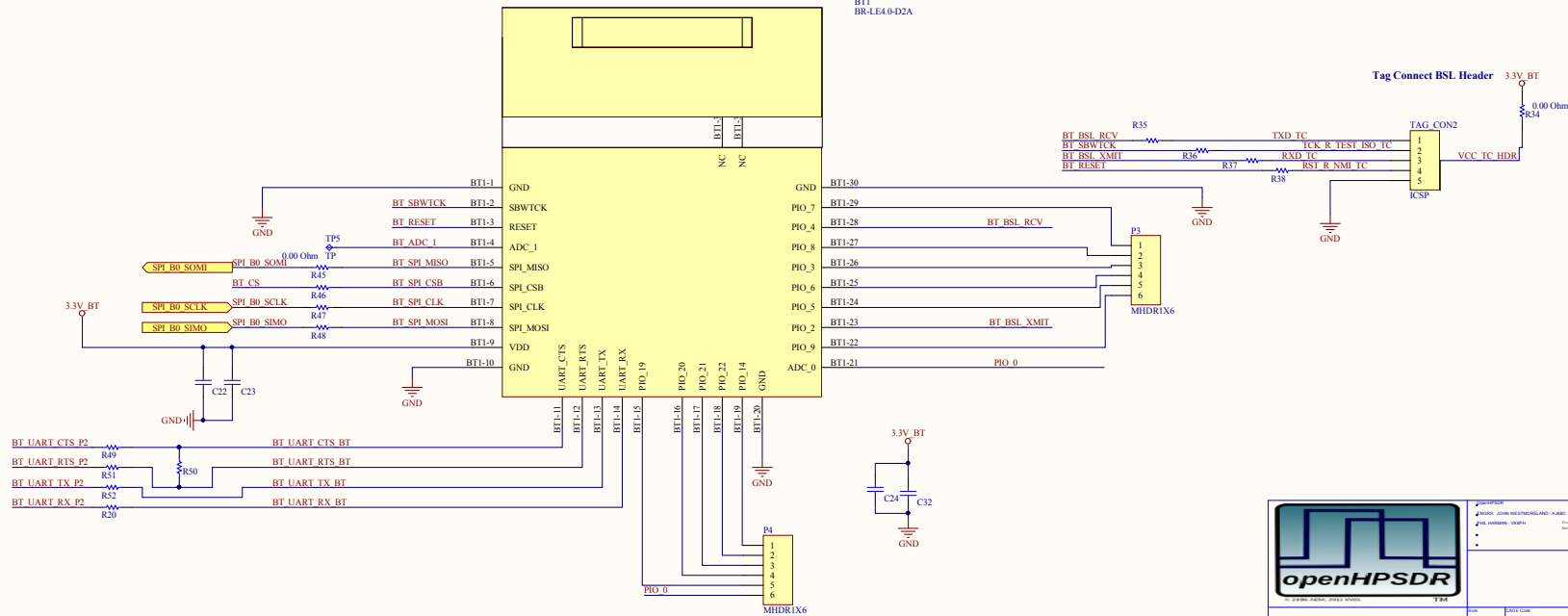
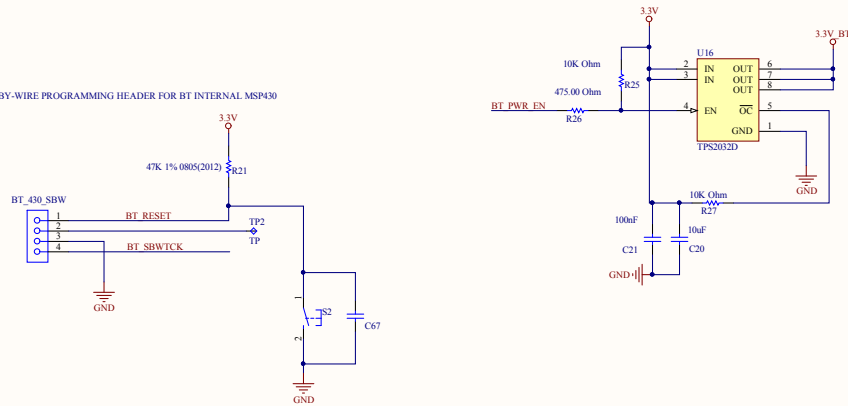
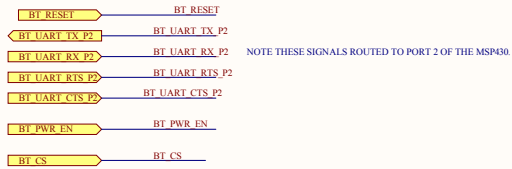
MICRO SD INTERFACE

Drawn By: John Westmoreland

Size	CAGE Code	DWG NO	Rev
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Scale	Date (Preliminary Schematic Release): May 10, 2014		Sheet
1/1 A			1 of 5

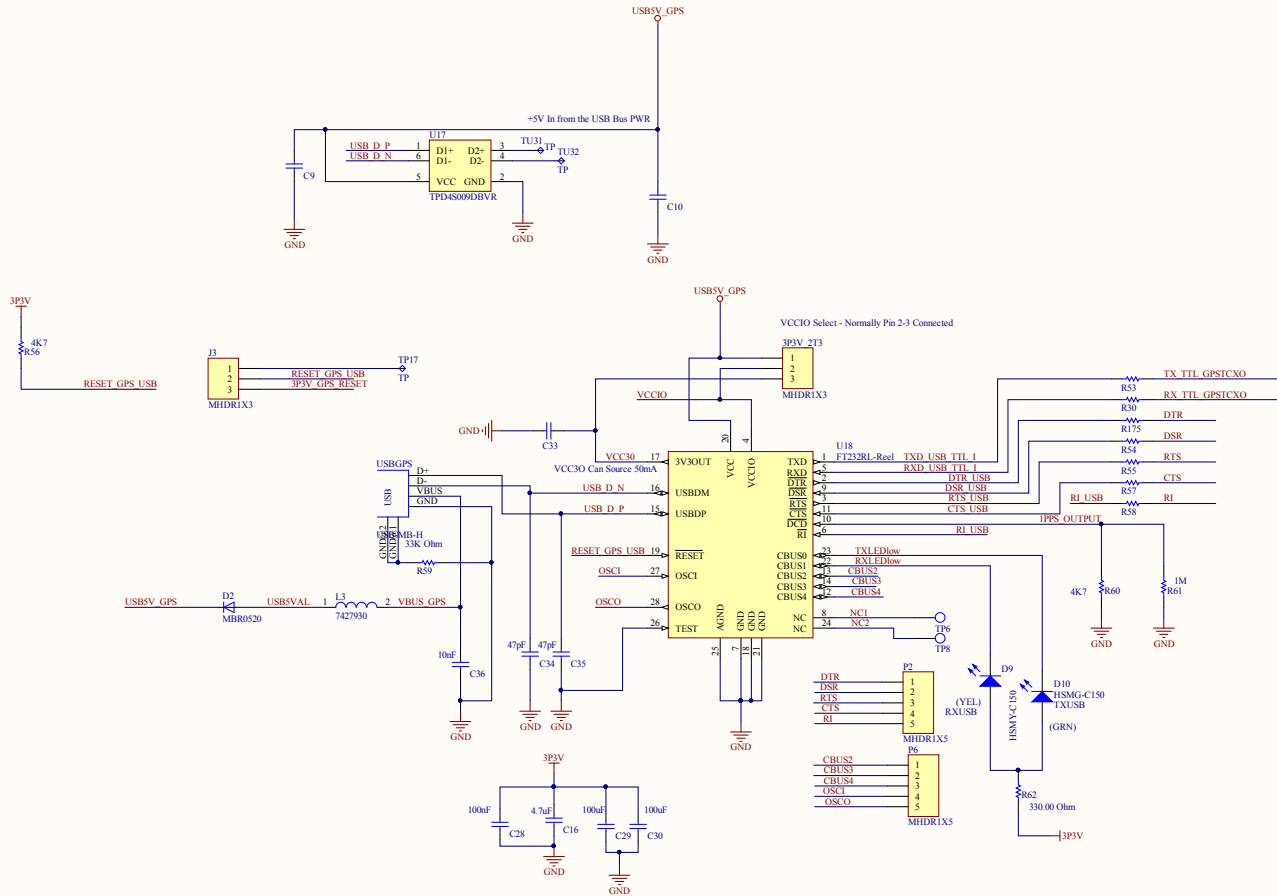


BLUETOOTH INTERFACE



TX USB TTL TX TTL GPSTCXO
 RX USB TTL RX TTL GPSTCXO
 1PPS IN GPS 1PPS OUTPUT
 RESET GPS USB 3P3V GPS_RESET

GPS USB INTERFACE



openHPSDR

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GPS USB INTERFACE

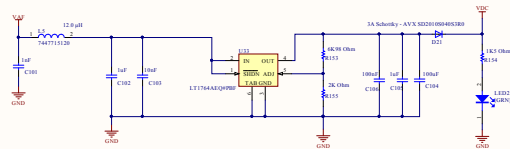
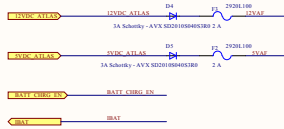
Version: 1.0

Author: John Westwood

Date: May 10, 2010

License: GPL

POWER DISTRIBUTION



PA Position	VAF	VDC	R1	R16	R18
2-3	12V	5V	1k5	4k78	2k
1-2	5V	3.3V	1k	4k12	2k

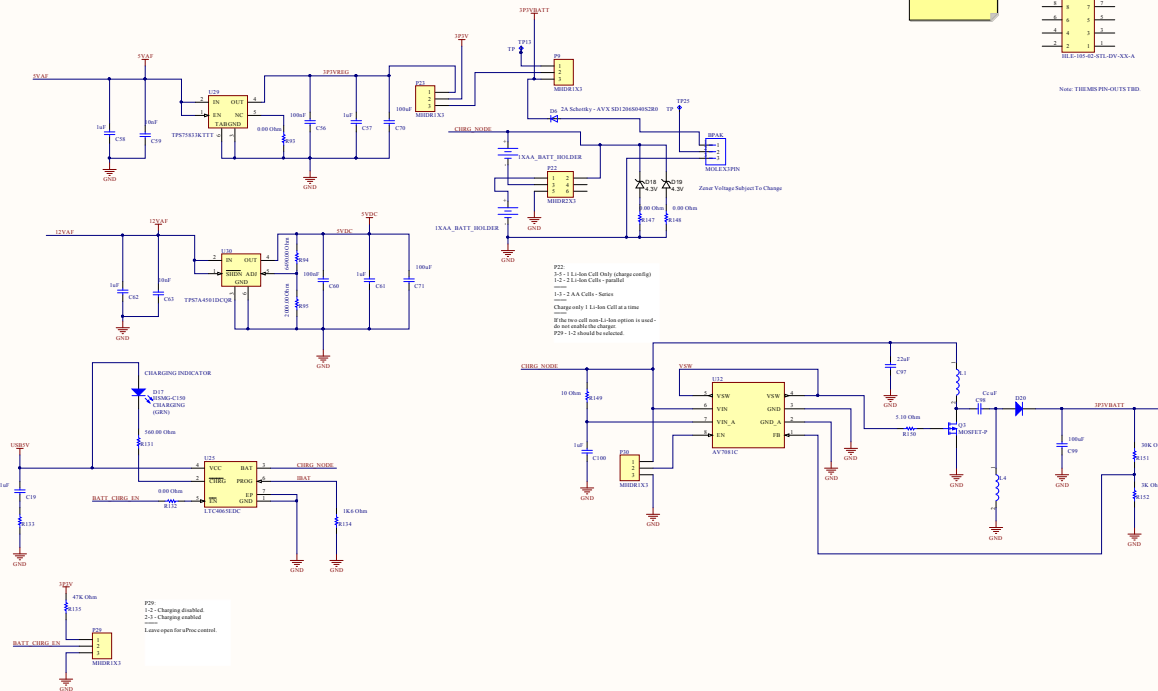
THEMIS CONNECTOR



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12	10	9	8	7	6	5	4	3	2	1

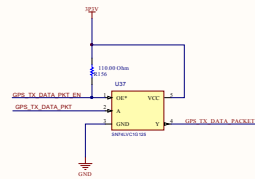
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12	10	9	8	7	6	5	4	3	2	1

Note: THEMIS PIN-OUTS TBD.



GPS_TX_DATA_PKT

GPS TX DATA PKT



		openHPSDR	
Project: openHPSDR		Version: 1.0.0	
Author: openHPSDR		License: GPL	
Copyright: 2008-2010		Date: 2010-10-10	
Project: openHPSDR		Version: 1.0.0	
Author: openHPSDR		License: GPL	
Copyright: 2008-2010		Date: 2010-10-10	